The listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1.-21. (Canceled)

22. (Previously Presented) A write-once memory device comprising:

a first memory cell formed over an insulating surface, and comprising a first semiconductor film having at least two first impurity regions and a first region therebetween, a first insulating film over the first semiconductor film, a first gate electrode formed over the first region, and at least two first wirings connected to the respective first impurity regions; and

a second memory cell formed over the insulating surface, and comprising a second semiconductor film having at least two second impurity regions and a second region therebetween, a second insulating film over the second semiconductor film, a second gate electrode formed over the second region, and at least two second wirings connected to the respective second impurity regions,

wherein the first region is altered to an insulating state and the second region is maintained in an initial state when applying a gate voltage to the first gate electrode and the second gate electrode, a first voltage to at least one of the two first wirings, and a second voltage to at least one of the two second wirings, and

wherein the first voltage is lower than the second voltage.

23. (New) The write-once memory device according to claim 22, further comprising sidewalls formed on side surfaces of the first gate electrode.

24. (New) The write-once memory device according to claim 22, further comprising sidewalls formed on side surfaces of the second gate electrode.

25. (New) The write-once memory device according to claim 22, further comprising sidewalls formed on side surfaces of each of the first gate electrode and the second gate electrode.

26. (New) A write-once memory device comprising:

a first memory cell formed over an insulating surface, and comprising a first semiconductor film comprising at least three first impurity regions, a first region, and a second region, a first insulating film over the first semiconductor film, a first gate electrode formed over the first region, a second gate electrode formed over the second region, and at least two first wirings connected to the respective first impurity regions, and

a second memory cell formed over the insulating surface, and comprising a second semiconductor film comprising at least three second impurity regions, a third region, and a fourth region, a second insulating film over the second semiconductor film, a third gate electrode formed over the third region, a fourth gate electrode formed over the fourth region, and at least two second wirings connected to the respective second impurity regions,

wherein the first region is altered to an insulating state and the third region is maintained in an initial state when applying a gate voltage to the first gate electrode and the third gate electrode, a first voltage to at least one of the two first wirings, and a second voltage to at least one of the two second wirings,

wherein the first voltage is lower than the second voltage,

wherein each of the first region and the second region is formed between the first impurity regions, and

wherein each of the third region and the fourth region is formed between the second impurity regions.

27. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of the first gate electrode.

28. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of the second gate electrode.

29. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of each of the first gate electrode and the second gate electrode.

30. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of the third gate electrode.

31. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of the fourth gate electrode.

32. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of each of the third gate electrode and the fourth gate electrode.

33. (New) The write-once memory device according to claim 26, further comprising sidewalls formed on side surfaces of each of the first gate electrode, the second gate electrode, the third gate electrode, and the fourth gate electrode.